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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/837,734	04/17/2001	Takaaki Nagai	NECF 18.591	9062

26304 7590 05/06/2003

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EXAMINER

OWENS, DOUGLAS W

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/837,734	NAGAI, TAKAAKI
	Examiner Douglas W Owens	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 14 February 2003.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1,2 and 5-18 is/are pending in the application.

4a) Of the above claim(s) 9-18 is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1,2 and 5-8 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on 14 February 2003 is: a) approved b) disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.

2. Certified copies of the priority documents have been received in Application No. _____.

3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on February 19, 2003 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.
2. The Patent and Trademark Office no longer makes drawing changes. See 1017 O.G. 4. It is applicant's responsibility to ensure that the drawings are corrected. Corrections must be made in accordance with the instructions below.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities -- 37 CFR 1.85

New corrected drawings must be filed with the changes incorporated therein. Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and centered within the top margin. If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings **MUST** be filed within the **THREE MONTH** shortened statutory period set for reply in the "Notice of Allowability." Extensions of time may NOT be obtained under the provisions of 37 CFR 1.136 for filing the corrected drawings after the mailing of a Notice of Allowability. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

2. Corrections other than Informalities Noted by Draftsperson on form PTO-948.

All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the same manner as above except that, normally, a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

Timing of Corrections

Applicant is required to submit acceptable corrected drawings within the time period set in the Office action. See 37 CFR 1.185(a). Failure to take corrective action within the set (or extended) period will result in **ABANDONMENT** of the application.

Claim Objections

3. Claim 2 is objected to because of the following informalities: in line 16, the word "in" should be replaced with "on". Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
5. Claims 7 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
6. Claims 7 and 8 depend from claims 3 and 4 respectively. The scope of the claims is not clear since claims 3 and 4 do not exist in the application.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1, 2 and 5 – 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 5,445,983 to Hong in view of US patent No. 6,091,634 to Wong.

Regarding claim 1, Hong teaches a non-volatile semiconductor storage apparatus comprising:

a memory cell field effect transistor having a floating gate (42) and a control gate (46);

a tunneling gate oxide layer (36) below the floating gate;

a select field effect transistor (24) having a drain (39) connected to a source of the memory cell field effect transistor; and

said floating gate extending to a position above the gate of the select transistor, wherein top and bottom surfaces of the floating gate and the control gate are parallel to top and bottom surfaces of the gate of the select field effect transistor.

Hong does not teach an array of storage cells. Wong teaches an array of storage cells (Fig. 1). It would have been obvious to one of ordinary skill in the art to incorporate the array of memory cells taught by Wong into the device taught by Hong since it is necessary to form an array in order to make a useful memory device.

Regarding claim 2, Hong teaches a non-volatile semiconductor storage apparatus having a memory cell field effect transistor and a select field effect transistor, said memory cell field effect transistor having a floating gate (42) and a control gate (46), a tunnel gate oxide layer (36) below the floating gate the select field effect transistor having a drain (39) connected to a source of the memory cell FET, said storage apparatus comprising:

a first semiconductor layer composing a portion of the floating gate and a gate of the select field effect transistor (the lower portion of the floating gate (42) is in the same layer of the device as the select gate (24);

an upper portion (second layer) of the floating gate (42) above a lower portion (first layer), said second portion not contacting the tunnel oxide, the upper portion (second layer) having a lower surface located at a height at least equal to a height of an upper surface of the lower portion (first layer), said second portion (second layer) extending to a position above the select gate (note: since the first and second layers comprise the same material, the only difference is in the method of production.

Therefore, the floating gate of Hong can be split into portions and considered two layers);

a first insulation layer (41) which insulates the select gate from the floating gate, said first insulation layer contacting said first semiconductor layer;

a second insulation layer (45) formed on the second semiconductor layer (second portion);

a third semiconductor layer (46) on the second insulation layer and composing said control gate; and

the third semiconductor layer, the second insulation layer, and the second semiconductor layer being etched using a single photoresist film (47; Fig. 3L).

Hong does not teach an array of storage cells. Wong teaches an array of storage cells (Fig. 1). It would have been obvious to one of ordinary skill in the art to

incorporate the array of memory cells taught by Wong into the device taught by Hong since it is necessary to form an array in order to make a useful memory device.

Regarding claims 5 and 6, Hong does not teach a drain diffusion layer shared between adjacent memory cell field effect transistors in a first direction in said unit cells. Wong teaches a drain diffusion layer shared between adjacent memory cell field effect transistors in a first direction in said unit cells. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Wong into the device taught by Hong for reasons discussed above.

Regarding claims 7 and 8, in so far as indefinite claims can be understood, Hong does not teach a drain diffusion shared between adjacent memory cell field effect transistors in a second direction in said unit cells. Wong teaches a drain diffusion layer shared between adjacent memory cell field effect transistors in a second direction in said unit cells. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Wong into the device taught by Yang for reasons discussed above.

Response to Arguments

9. Applicant's arguments with respect to claims 1, 2 and 5 – 9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 703-308-6167. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

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DWO
April 30, 2003

Tom Thomas
TOM THOMAS
SUPERVISORY PATENT EXAMINER
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